UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,756	07/24/2003	Kevin Traynor	032674-200	1739

7590 01/13/2006

Burns, Doane, Swecker & Mathis, L.L.P.
P.O. Box 1404
Alexandria, VA 22313-1404

EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 01/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,756	TRAYNOR ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-20* is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/4/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 14-20 are allowed.

2. The following is an examiner's statement of reasons for allowance:

Referring to claim 14: The prior arts applied in the rejection on record do not explicitly disclose presence of the interrupt request. The claim recites the limitations of the structures for sharing a plurality of interrupt inputs comprising, for each interrupt input, a plurality of logical AND gates, each corresponding to an interrupt source, a plurality of control bits, each corresponding to an interrupt source, and a logical OR gate to indicate, to the interrupt input, the presence of a corresponding interrupt request signal from at least one output of the plurality of logical AND gates. The structure shown in Figure 6 of the Prenn patent does not function to indicate the presence of an interrupt request signal to the interrupt input, as recited in claim 14. Rather, this structure corresponds to the product term generator 252, summary term generator 206, and selection circuit 208 shown in Figure 2 of the patent. The output of these circuits comprises a maximum value signal MV on line 152. In contrast, the interrupt request signal IRQ that is sent to an interrupt input is produced by the request logic 204. It can be seen from Figure 2 that the circuits 252, 206 and 208 are not involved in the generation of the interrupt request. Among other distinctions, therefore, the logical OR gates 632-636 in Figure 6 do not indicate "to the interrupt input" the presence of an interrupt request signal, as recited in claim 14. Rather, they each produce a summary term bit ST that is provided to the selector circuit.

Referring to claims 15-20: Claims are allowable because they incorporate the parent claim's allowable subject matter.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-3, 6-9, and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Suh (U.S. Patent No. 6,742,065) and Prenn (U.S. Patent No. 6,734,984).

Referring to claim 1: Suh discloses an interrupt controller and a method of accessing interrupts. Suh discloses mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs (figure 3, connections between structures 30 and 40, and between structures 30 and 50). Suh discloses control logic (figure 1, structure 90) to enable and to disable the interrupt controller, but Suh does not explicitly discloses selectively enabling interrupt requests from each of the plurality of interrupt sources to one or more of the plurality of interrupt inputs.

Prenn discloses an interrupt handling circuit. Prenn discloses a "PARTICIPATE" signal to selectively enable or to selectively disable the associated interrupt signal (figure 6, signals go into structure 601, column 8, last paragraph, and column 9, lines 1-8); Prenn's "PARTICIPATE" signals are the control bits. Each of Prenn's "PARTICIPATE" signals attaches to the AND gate between each of the plurality of interrupt sources and one of the interrupt inputs. Prenn teaches one to implement a system with priority setting over each interrupt source and a system design with expandability, less added complexity, and less added propagation delay (column 2, lines 50-52, and column 9, line 12).

Hence, it would have been obvious to one having ordinary skill in the computer art to adopt Prenn's teaching onto Suh at the time Applicant made the invention because Prenn teaches one to implement a system with priority setting over each interrupt source and a system design with expandability, less added complexity, and less added propagation delay.

Referring to claim 2: Prenn generates the "PARTICIPATE" signals via a comparator (figure 2, structure 248); the comparator's comparing operation is the claimed determining a value of control bits respectively associated with each mapped interrupt source/interrupt input

combination. Prenn discloses that only selected number of item generators of array (figure 2, structure 202) will output signals based on the "PARTICIPATE" signal (column 8, lines 60-67), which is the claimed selectively enabling interrupt requests between the mapped interrupt source/interrupt input combination according to the respective control bit values.

Referring to claim 3: Prenn generates the "PARTICIPATE" signals via a comparator (figure 2, structure 248); the comparator's comparing operation is the claimed determining a value of control bits respectively associated with each mapped interrupt source/interrupt input combination. Prenn discloses that only selected number of item generators of array (figure 2, structure 202) will output signals based on the "PARTICIPATE" signal (column 8, lines 60-67), which is the claimed selectively enabling interrupt requests between the mapped interrupt source/interrupt input combination according to the respective control bit values. Furthermore, each of Prenn's interrupt request processing blocks (figure 2, structures 224, 226, and 228) has a comparator for generating "PARTICIPATE" signal; thus Prenn discloses repeating the steps of determining value for each combination and selectively enabling interrupt requests until every interrupt source/interrupt input combination is handled.

Referring to claim 6: Prenn teaches one to implement a system with priority setting (column 9, line 12), which is the claimed defining control bit values according to the system requirement.

Referring to claim 7: Suh discloses an interrupt controller and a method of accessing interrupts. Suh discloses mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs (figure 3, connections between structures 30 and 40, and between structures 30 and 50). Suh discloses control logic (figure 1, structure 90) to enable and to disable

the interrupt controller, but Suh does not explicitly discloses selectively enabling interrupt requests from each of the plurality of interrupt sources to one or more of the plurality of interrupt inputs.

Prenn discloses an interrupt handling circuit. Prenn discloses a "PARTICIPATE" signal to selectively enable or to selectively disable the associated interrupt signal (figure 6, signals go into structure 601, column 8, last paragraph, and column 9, lines 1-8); Prenn's "PARTICIPATE" signals are the control bits. Each of Prenn's "PARTICIPATE" signals attaches to the AND gate between each of the plurality of interrupt sources and one of the interrupt inputs. Prenn teaches one to implement a system with priority setting over each interrupt source and a system design with expandability, less added complexity, and less added propagation delay (column 2, lines 50-52, and column 9, line 12).

Hence, it would have been obvious to one having ordinary skill in the computer art to adopt Prenn's teaching onto Suh at the time Applicant made the invention because Prenn teaches one to implement a system with priority setting over each interrupt source and a system design with expandability, less added complexity, and less added propagation delay.

Referring to claim 8: Prenn generates the "PARTICIPATE" signals via a comparator (figure 2, structure 248); the comparator's comparing operation is the claimed determining a value of control bits respectively associated with each mapped interrupt source/interrupt input combination. Prenn discloses that only selected number of item generators of array (figure 2, structure 202) will output signals based on the "PARTICIPATE" signal (column 8, lines 60-67), which is the claimed selectively enabling interrupt requests between the mapped interrupt source/interrupt input combination according to the respective control bit values.

Referring to claim 9: Prenn generates the "PARTICIPATE" signals via a comparator (figure 2, structure 248); the comparator's comparing operation is the claimed determining a value of control bits respectively associated with each mapped interrupt source/interrupt input combination. Prenn discloses that only selected number of item generators of array (figure 2, structure 202) will output signals based on the "PARTICIPATE" signal (column 8, lines 60-67), which is the claimed selectively enabling interrupt requests between the mapped interrupt source/interrupt input combination according to the respective control bit values. Furthermore, each of Prenn's interrupt request processing blocks (figure 2, structures 224, 226, and 228) has a comparator for generating "PARTICIPATE" signal; thus Prenn discloses repeating the steps of determining value for each combination and selectively enabling interrupt requests until every interrupt source/interrupt input combination is handled.

Referring to claim 12: Prenn teaches one to implement a system with priority setting (column 9, line 12), which is the claimed defining control bit values according to the system requirement.

Referring to claim 13: Prenn discloses the AND gates (figure 6, AND gates in structure 601).

7. Claims 4-5 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Suh, Prenn, and Monahan et al. (U.S. Patent No. 4,001,783).

Referring to claims 4 and 10: Suh and Prenn's disclosures are stated above; neither of them explicitly discloses setting the control bit values according to user preference. Monahan discloses a priority interrupt mechanism, and Monahan discloses a programmable interface

application to configure interrupt related information, such as the priority (column 3, lines 10-14). Monahan teaches one to further adjust the system performance by customize priority for each interrupt request source. Hence, it would have been obvious to one having ordinary skill in the computer art to adopt Monahan's teaching onto Suh and Prenn because Monohan teaches one to implement a system with flexibility allowing user to further adjust the system performance by customize priority for each interrupt request source.

Referring to claims 5 and 11: Monahan discloses a programmable interface application for interrupt configuration, which configures the system while system is in operation. Thus, Monahan discloses dynamically modifying according to user preference.

Response to Arguments

8. In response to Applicant's argument that Suh does not disclose mapping each of the plurality of interrupt source to each of the plurality of interrupt inputs, and Prenn does not provide the selective enabling feature (Remark, page 4, 4th paragraph, page 5, 1st paragraph): Suh discloses that the pending register stores the requests and forwards the requests to the priority logic (figure 3). Suh discloses a plurality of interrupt requests (figure 3, is0...is25) and a plurality of connections to priority logic (connections between structures 30 and 40, and between structures 30 and 50). Thus, Suh does disclose mapping each of the plurality of interrupt sources to each of the plurality of interrupt inputs. Prenn discloses an interrupt handling circuit. Prenn discloses a "PARTICIPATE" signal to selectively enable or to selectively disable the associated interrupt signal (figure 6, signals go into structure 601, column 8, last paragraph, and column 9, lines 1-8); Prenn's "PARTICIPATE" signals are the control bits. Each of Prenn's

"PARTICIPATE" signals attaches to the AND gate between each of the plurality of interrupt sources and one of the interrupt inputs. Prenn teaches one to implement a system with priority setting over each interrupt source and a system design with expandability, less added complexity, and less added propagation delay (column 2, lines 50-52, and column 9, line 12). The language of the claimed limitations as drafted is too broad, and thus is insufficient to distinguish from the prior arts.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen

can be reached on 571-272-3676 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
January 4, 2006

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
1/9/2006